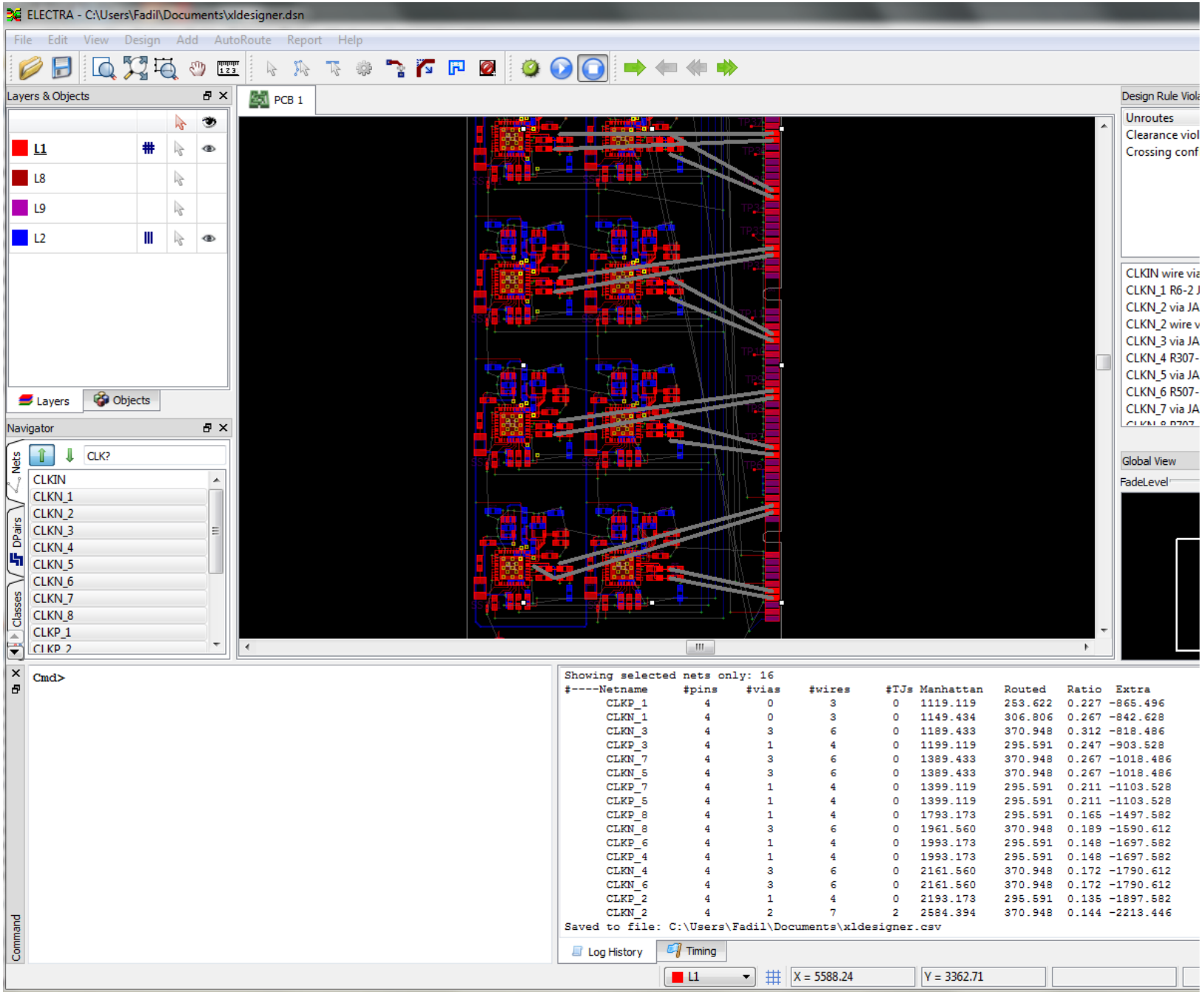
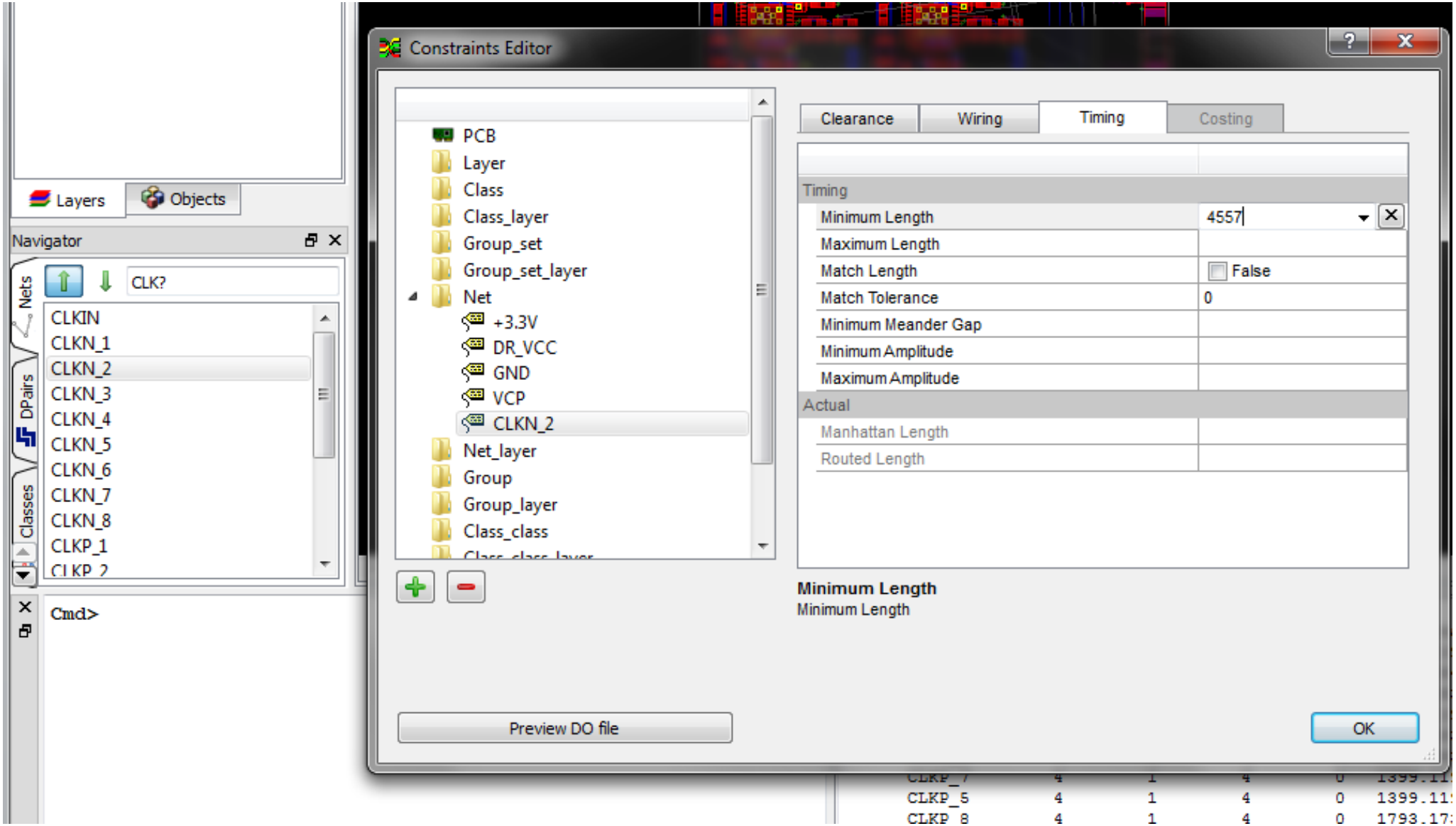
1. **Navigator Nets Panel, enter CLK? as filter and drag select all the CLK nets of interest**
2. **Once selected, invoke menu “Report Network”, length report is shown under the log panel. Compare with table.**

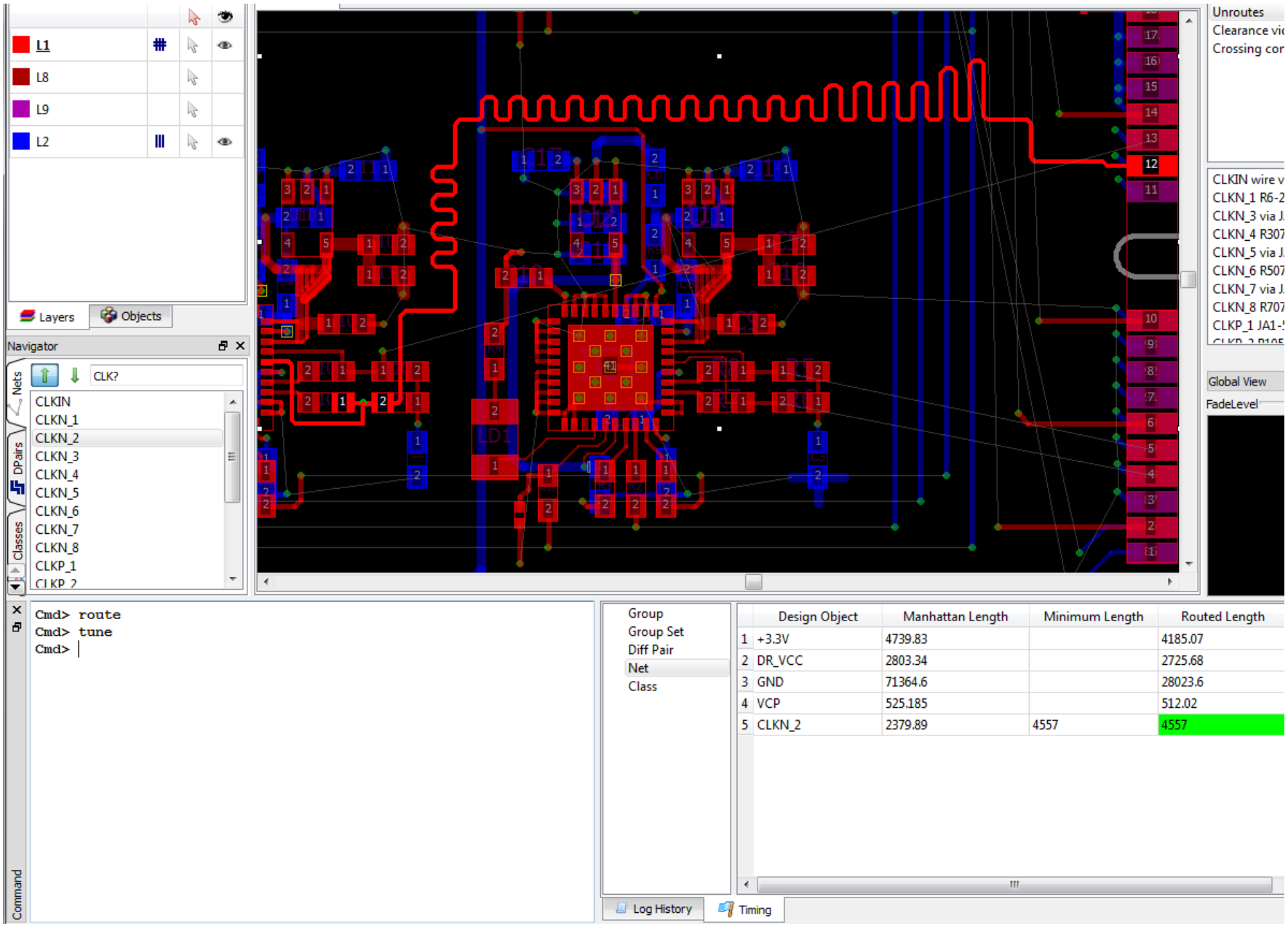


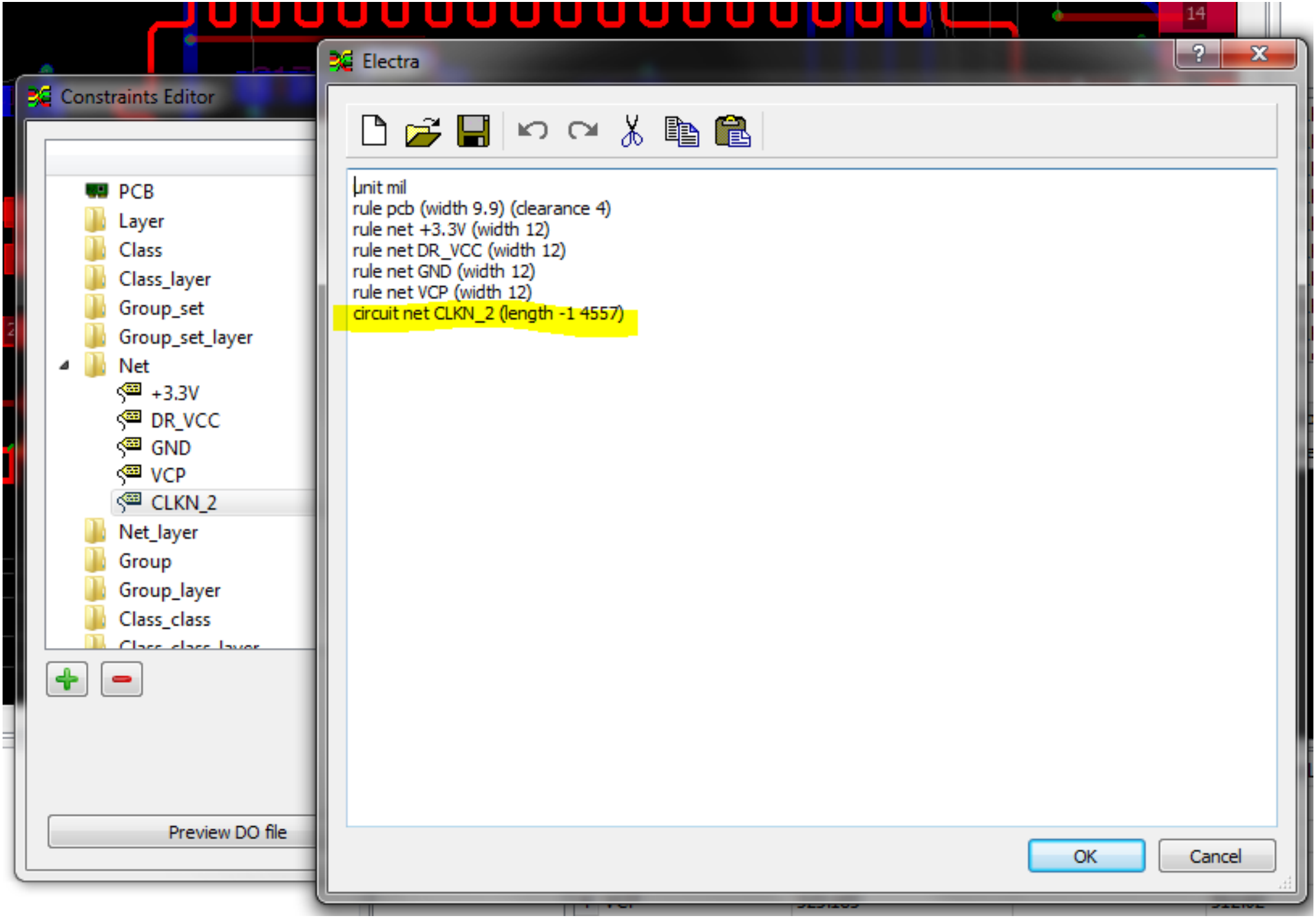
Invoke the Contraints Editor, select the Net branch and click on + button to add a net rule. Under Timing tab, enter a “Minimum Length” of 4557 (mil is current unit)

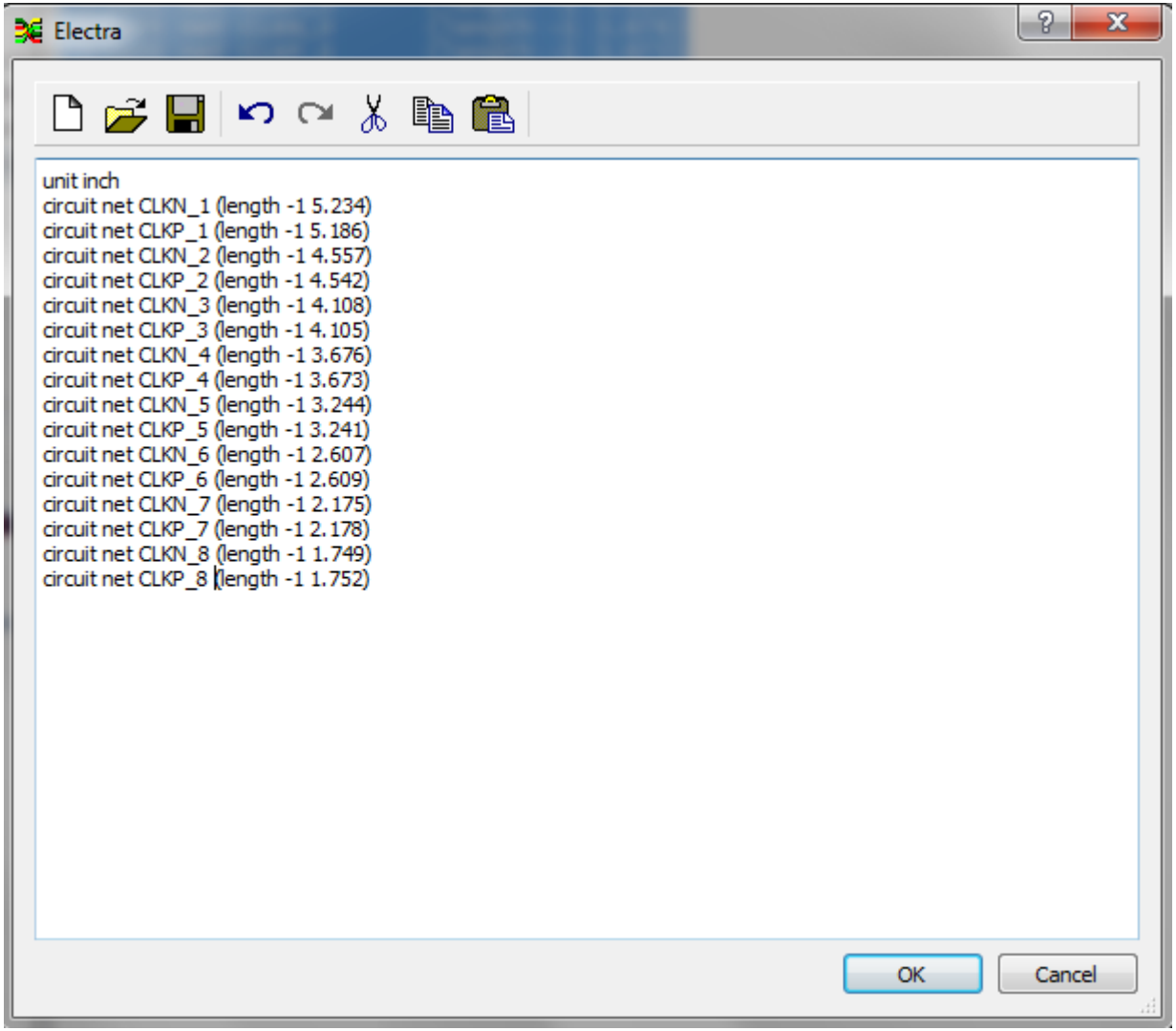


Type “route” in the command console. Serpentine is inserted to meet min length requirement. Select “Timing tab” and “Net” in the log panel.

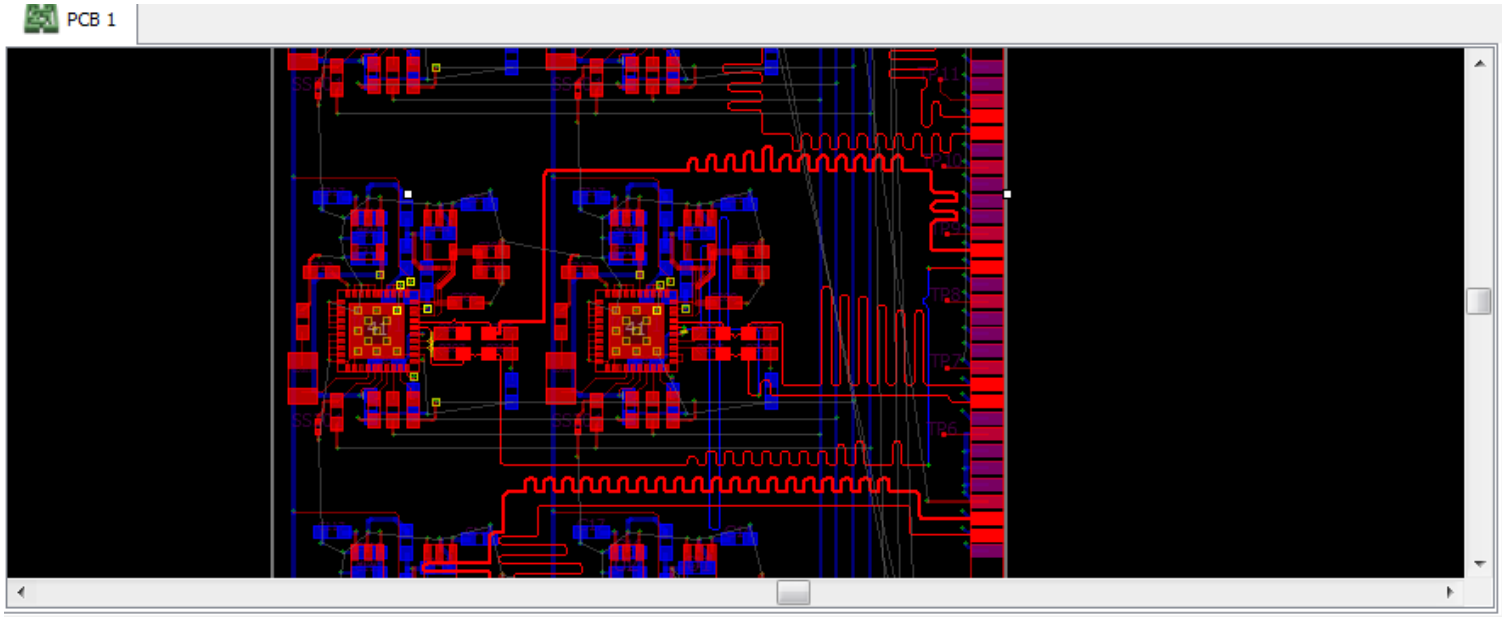
Type “tune” to refine.




Constraints Editor
PCB
Layer
Class
Class_layer
Group_set
Group_set_layer
Net
+3.3V
DR_VCC
GND
VCP
CLKN_2
Net_layer
Group
Group_layer
Class_class
Preview DO file
Electra
unit mil
rule pcb (width 9.9) (clearance 4)
rule net +3.3V (width 12)
rule net DR_VCC (width 12)
rule net GND (width 12)
rule net VCP (width 12)
circuit net CLKN_2 (length -1 4557)
OK
Cancel



CLK	LENGTH
CLKN1	5.234
CLKP1	5.186
CLKN2	4.557
CLKP2	4.542
CLKN3	4.108
CLKP3	4.105
CLKN4	3.676
CLKP4	3.673
CLKN5	3.244
CLKP5	3.241
CLKN6	2.607
CLKP6	2.609
CLKN7	2.175
CLKP7	2.178
CLKN8	1.749
CLKP8	1.752



Design Rule Violations

Unroutes (264)

Clearance violations

Crossing conflicts

CLKIN wire via
GND C10-2 C9-2
GND C10-2 JA1-94
GND C102-2 C103-2
GND C105-2 C110-2

AutoL

Global View

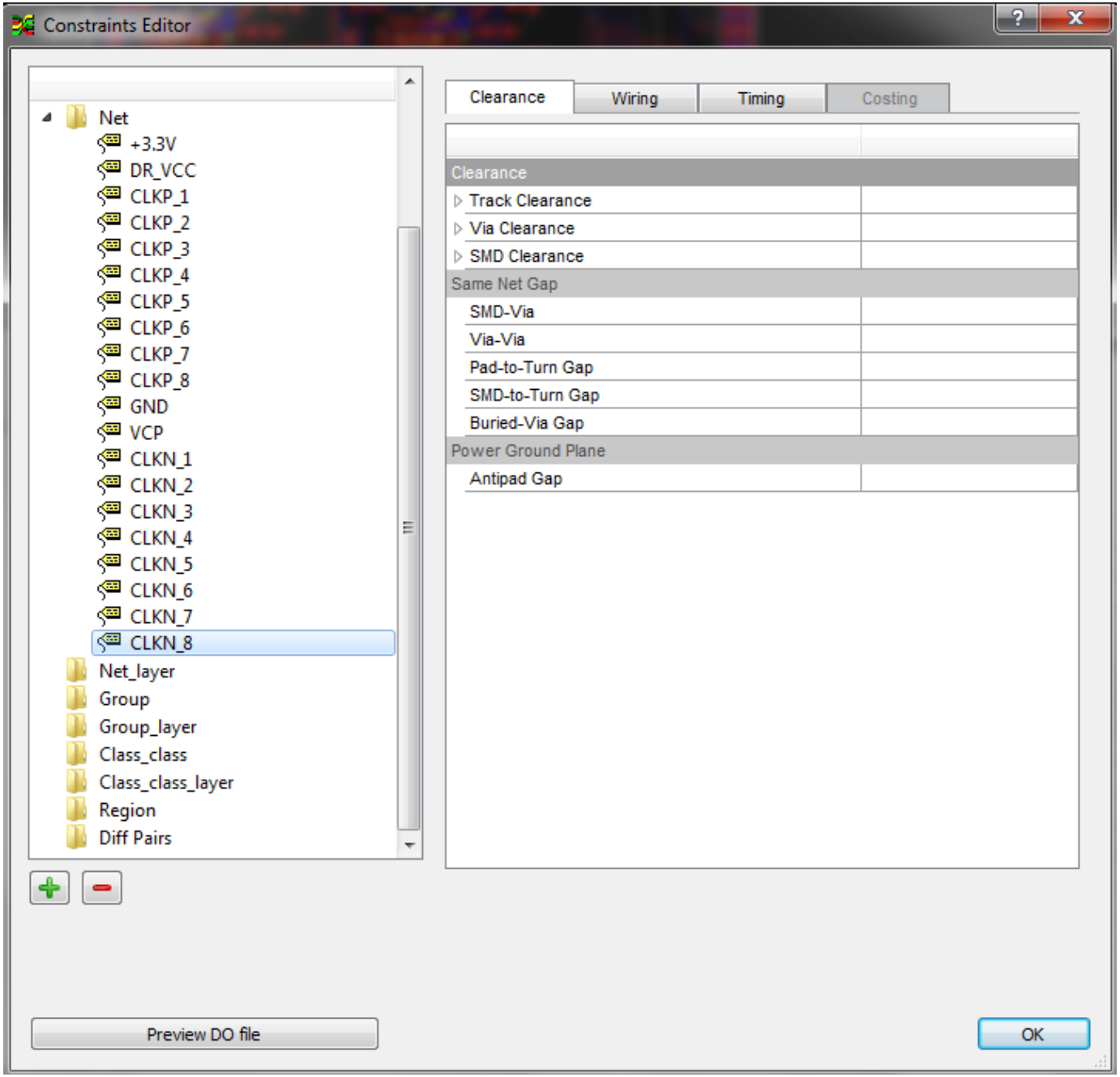
FadeLevel

Group
Group Set
Diff Pair
Net
Class

	Design Object	Manhattan Length	Minimum Length	Routed Length	Maximum Length	Match	Actual Tolerance
1	+3.3V	4.73983		4.19			
2	DR_VCC	2.80334		2.73			
3	CLKP_1	1.20502	5.186	1.19			-77.05%
4	CLKP_2	2.19317	4.542	4.18			-7.97%
5	CLKP_3	1.11912	4.105	4.1			-0.12%
6	CLKP_4	2.0309	3.673	3.67			-0.08%
7	CLKP_5	1.31912	3.241	3.24			-0.03%
8	CLKP_6	1.99317	2.609	2.61			0.04%
9	CLKP_8	1.79317	1.752	2.7			54.11%
10	CLKP_7	1.31912	2.178	2.18			0.09%
11	GND	68.0725		24.74			
12	VCP	0.525185		0.51			
13	CLKN_1	1.14943	5.234	3.6			-31.22%
14	CLKN_2	2.28349	4.557	4.56			0.07%
15	CLKN_3	1.37933	4.108	3.79			-7.74%
16	CLKN_4	2.70803	3.676	3.69			0.38%
17	CLKN_5	1.46751	3.244	3.26			0.49%
18	CLKN_6	2.68933	2.607	2.68			2.80%
19	CLKN_7	1.46751	2.175	2.19			0.69%
20	CLKN_8	2.62293	1.749	2.63			50.37%

Log History

Timing


Constraints Editor
Net
+3.3V
DR_VCC
CLKP_1
CLKP_2
CLKP_3
CLKP_4
CLKP_5
CLKP_6
CLKP_7
CLKP_8
GND
VCP
CLKN_1
CLKN_2
CLKN_3
CLKN_4
CLKN_5
CLKN_6
CLKN_7
CLKN_8
Net_layer
Group
Group_layer
Class_class
Class_class_layer
Region
Diff Pairs
Clearance
Wiring
Timing
Costing
Clearance
Track Clearance
Via Clearance
SMD Clearance
Same Net Gap
SMD-Via
Via-Via
Pad-to-Turn Gap
SMD-to-Turn Gap
Buried-Via Gap
Power Ground Plane
Antipad Gap
Preview DO file
OK