

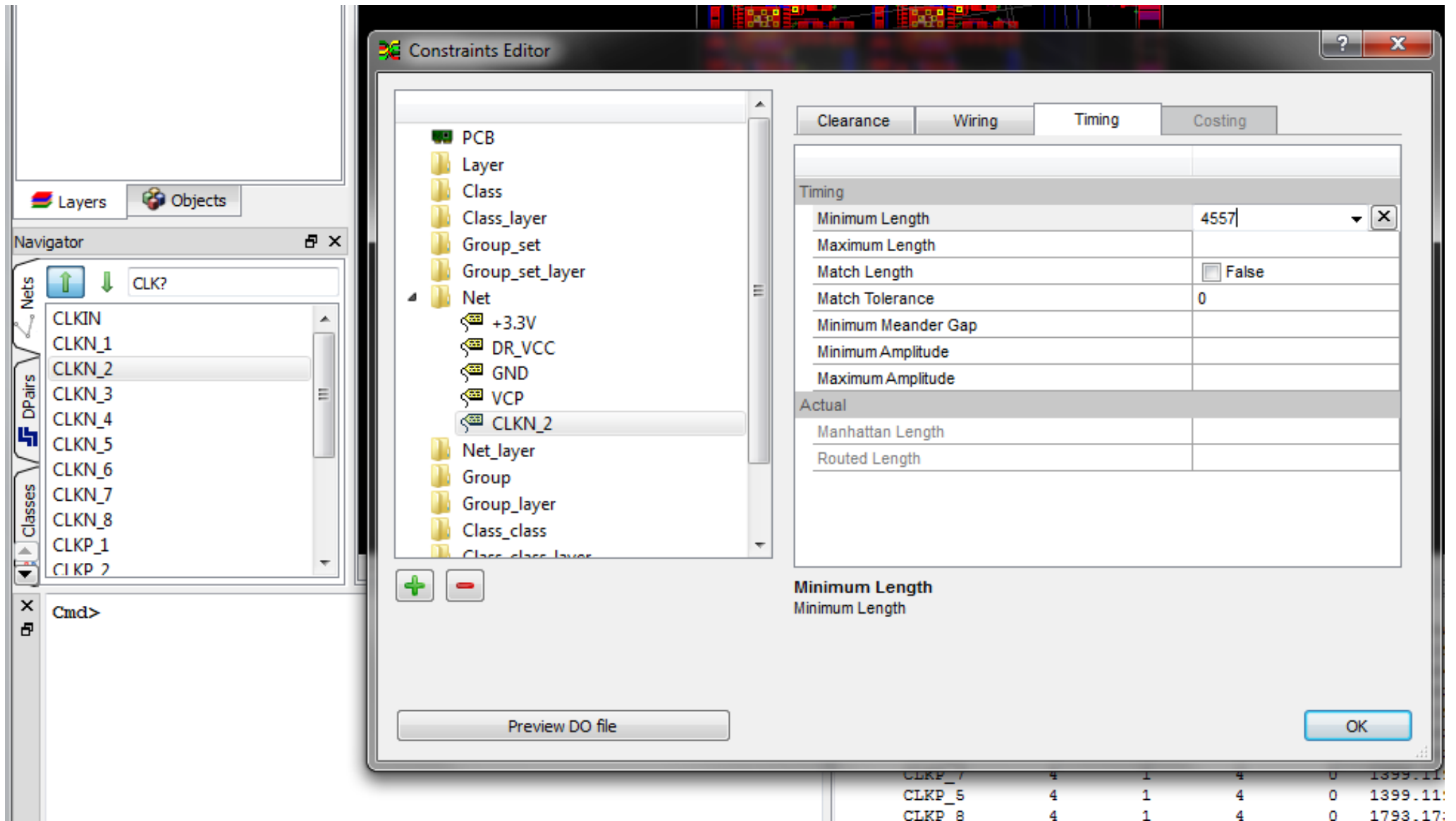
1. Navigator Nets Panel, enter CLK? as filter and drag select all the CLK nets of interest
2. Once selected, invoke menu "Report Network", length report is shown under the log panel. Compare with table.

The screenshot shows the ELECTRA PCB design software interface. The main window displays a PCB layout with various components and routing. The Navigator Nets Panel is filtered with 'CLK?' and shows a list of selected nets. The Command window displays a network report table with columns for Netname, #pins, #vias, #wires, #TJs, Manhattan, Routed, Ratio, and Extra. The report lists 16 selected nets and their associated metrics.

#	Netname	#pins	#vias	#wires	#TJs	Manhattan	Routed	Ratio	Extra
1	CLKP_1	4	0	3	0	1119.119	253.622	0.227	-865.496
2	CLKN_1	4	0	3	0	1149.434	306.806	0.267	-842.628
3	CLKN_3	4	3	6	0	1189.433	370.948	0.312	-818.486
4	CLKP_3	4	1	4	0	1199.119	295.591	0.247	-903.528
5	CLKN_7	4	3	6	0	1389.433	370.948	0.267	-1018.486
6	CLKN_5	4	3	6	0	1389.433	370.948	0.267	-1018.486
7	CLKP_7	4	1	4	0	1399.119	295.591	0.211	-1103.528
8	CLKP_5	4	1	4	0	1399.119	295.591	0.211	-1103.528
9	CLKP_8	4	1	4	0	1793.173	295.591	0.165	-1497.582
10	CLKN_8	4	3	6	0	1961.560	370.948	0.189	-1590.612
11	CLKP_6	4	1	4	0	1993.173	295.591	0.148	-1697.582
12	CLKP_4	4	1	4	0	1993.173	295.591	0.148	-1697.582
13	CLKN_4	4	3	6	0	2161.560	370.948	0.172	-1790.612
14	CLKN_6	4	3	6	0	2161.560	370.948	0.172	-1790.612
15	CLKP_2	4	1	4	0	2193.173	295.591	0.135	-1897.582
16	CLKN_2	4	2	7	2	2584.394	370.948	0.144	-2213.446

Saved to file: C:\Users\Fadi\Documents\xl designer.csv

Invoke the Constraints Editor, select the Net branch and click on + button to add a net rule. Under Timing tab, enter a "Minimum Length" of 4557 (mil is current unit)



Type "route" in the command console. Serpentine is inserted to meet min length requirement. Select "Timing tab" and "Net" in the log panel.

Type "tune" to refine.

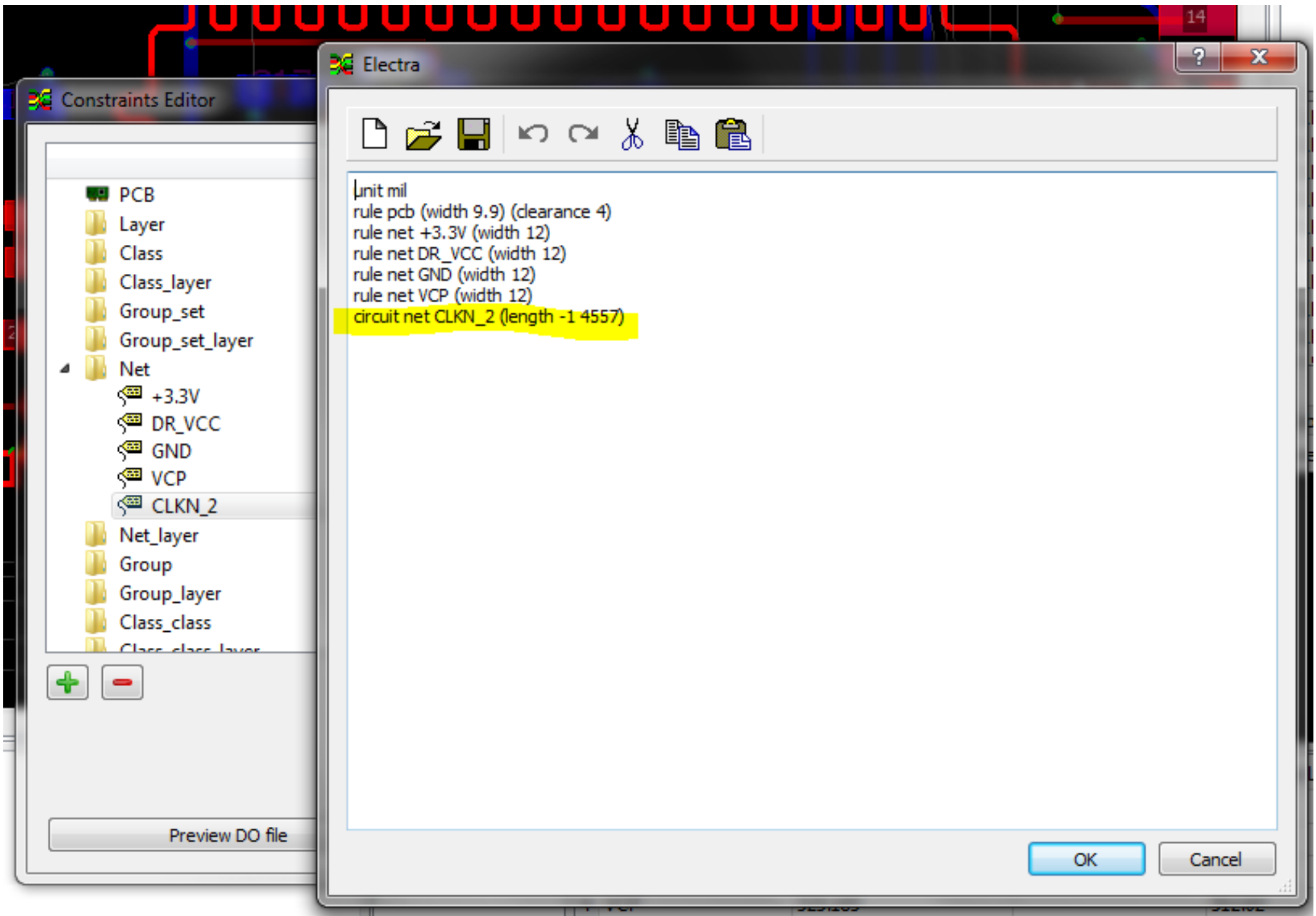
The screenshot displays a PCB design tool interface. On the left, a layer legend shows L1 (red), L8 (dark red), L9 (purple), and L2 (blue). Below it is a Navigator panel with a tree view showing 'Nets' and 'Classes'. The 'Nets' list includes CLKIN, CLKN_1 through CLKN_8, and CLKP_1 through CLKP_2. The 'Classes' list includes CLKN_2. The main workspace shows a complex routing layout with a prominent red serpentine pattern for net CLKN_2. On the right, a 'Unroutes' panel lists various routing objects. Below that, a 'Global View' panel shows a 'FadeLevel' slider. At the bottom, a Command console shows the following commands:

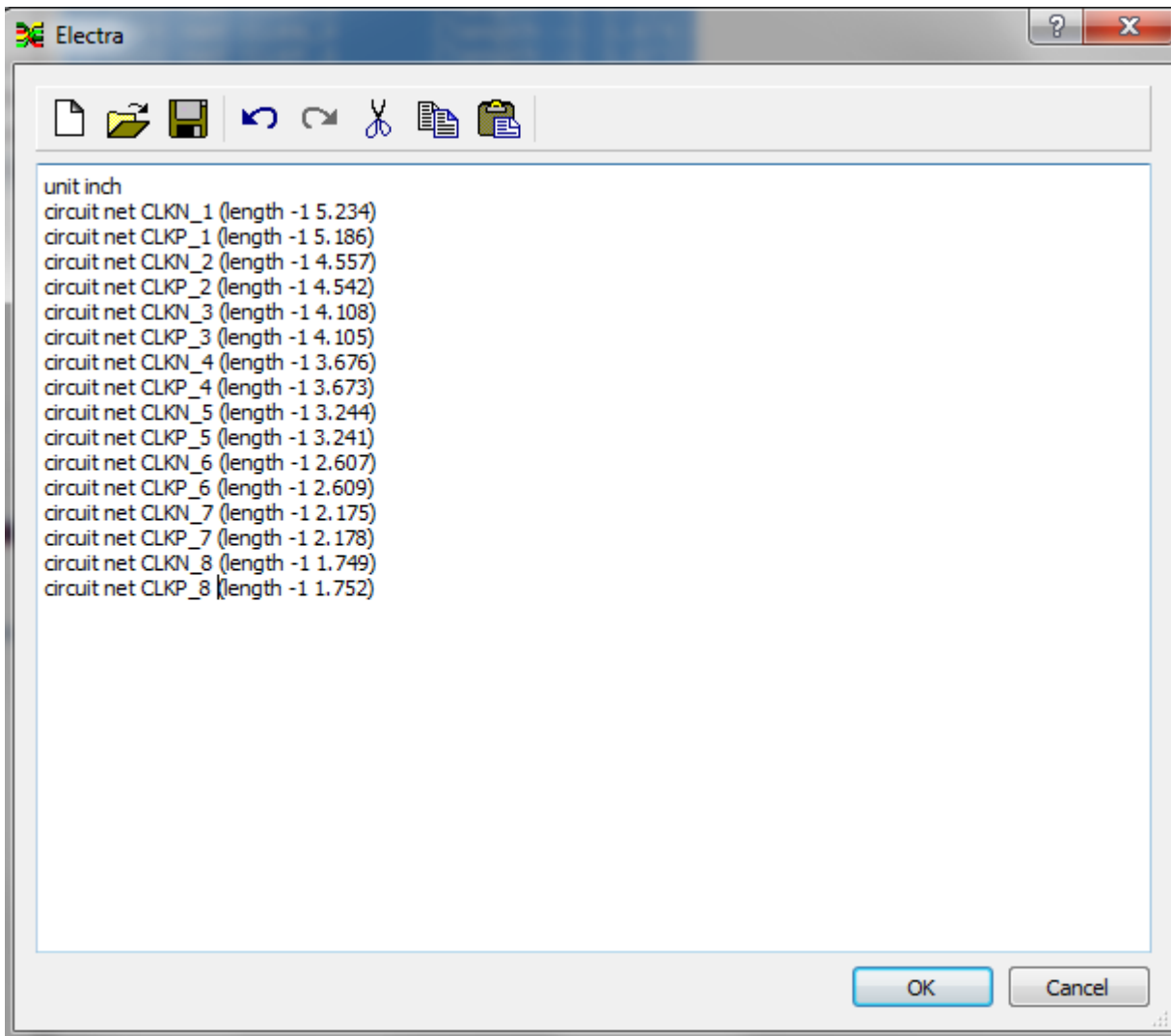
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Cmd> route
Cmd> tune
Cmd> |
```

Below the command console is a table with the following data:

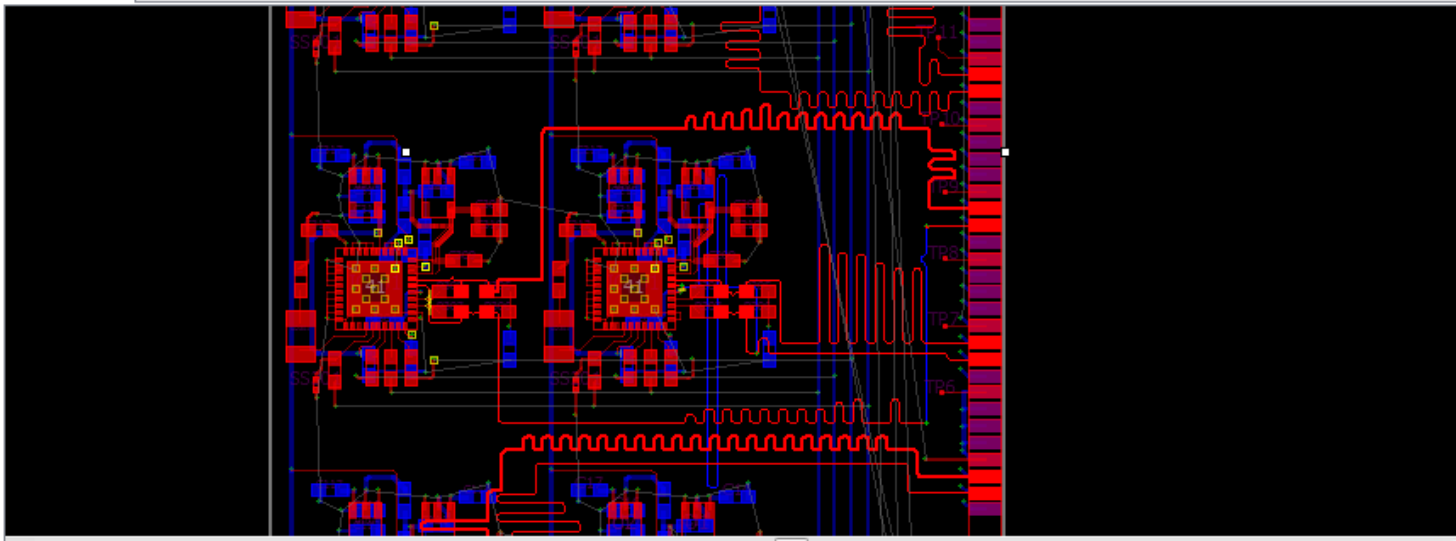
Group	Design Object	Manhattan Length	Minimum Length	Routed Length
1	+3.3V	4739.83		4185.07
2	DR_VCC	2803.34		2725.68
3	GND	71364.6		28023.6
4	VCP	525.185		512.02
5	CLKN_2	2379.89	4557	4557

At the bottom of the interface, there are buttons for 'Log History' and 'Timing'.





CLK	LENGTH
CLKN1	5.234
CLKP1	5.186
CLKN2	4.557
CLKP2	4.542
CLKN3	4.108
CLKP3	4.105
CLKN4	3.676
CLKP4	3.673
CLKN5	3.244
CLKP5	3.241
CLKN6	2.607
CLKP6	2.609
CLKN7	2.175
CLKP7	2.178
CLKN8	1.749
CLKP8	1.752



Design Rule Violations

Unroutes (264)
 Clearance violations
 Crossing conflicts

CLKIN wire via
 GND C10-2 C9-2
 GND C10-2 JA1-94
 GND C102-2 C103-2
 GND C105-2 C110-2

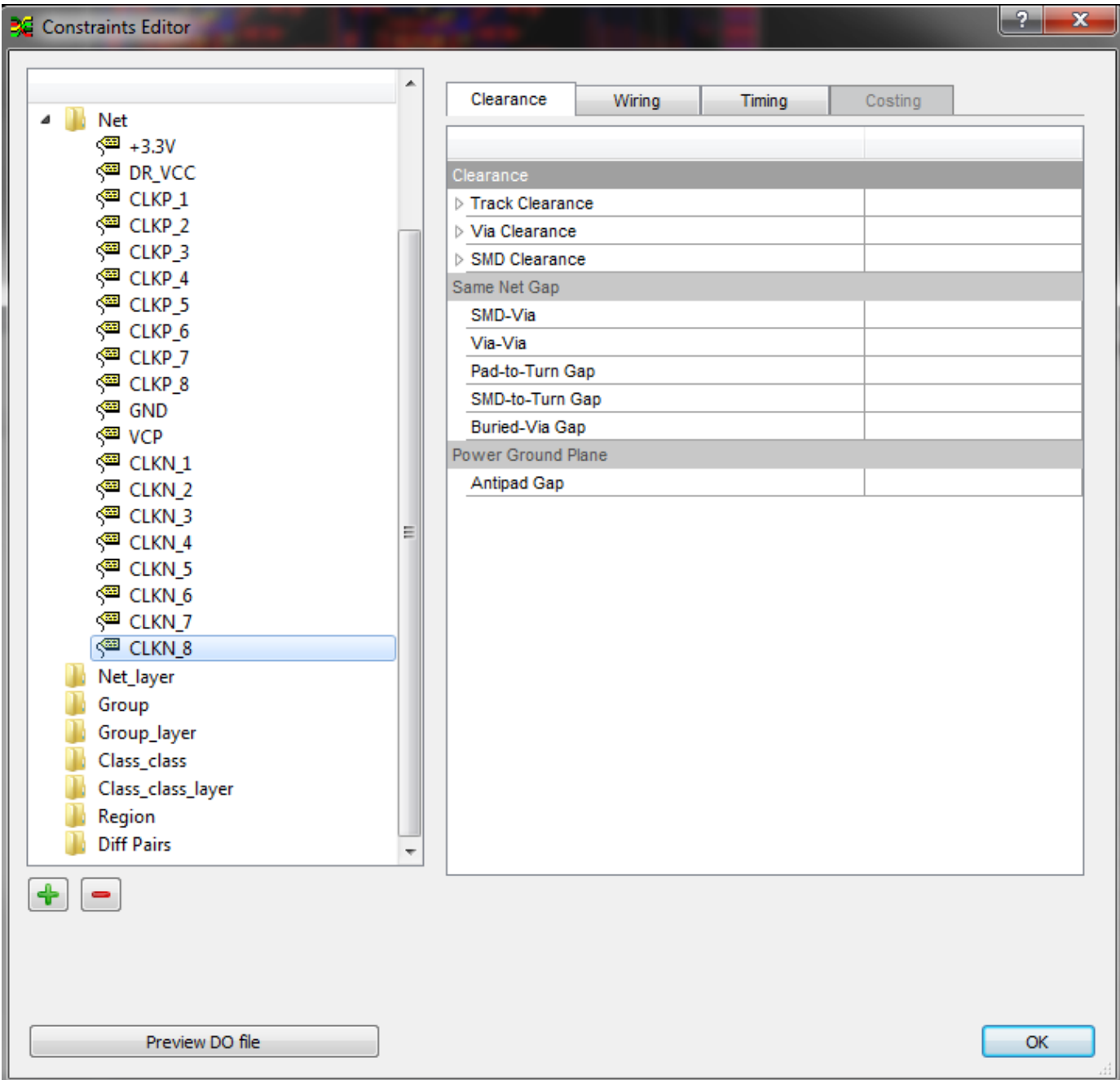
AutoL

Global View

FadeLevel



Group	Design Object	Manhattan Length	Minimum Length	Routed Length	Maximum Length	Match	Actual Tolerance
Group Set	1 +3.3V	4.73983		4.19			
Diff Pair	2 DR_VCC	2.80334		2.73			
Net	3 CLKP_1	1.20502	5.186	1.19			-77.05%
Class	4 CLKP_2	2.19317	4.542	4.18			-7.97%
	5 CLKP_3	1.11912	4.105	4.1			-0.12%
	6 CLKP_4	2.0309	3.673	3.67			-0.08%
	7 CLKP_5	1.31912	3.241	3.24			-0.03%
	8 CLKP_6	1.99317	2.609	2.61			0.04%
	9 CLKP_8	1.79317	1.752	2.7			54.11%
	10 CLKP_7	1.31912	2.178	2.18			0.09%
	11 GND	68.0725		24.74			
	12 VCP	0.525185		0.51			
	13 CLKN_1	1.14943	5.234	3.6			-31.22%
	14 CLKN_2	2.28349	4.557	4.56			0.07%
	15 CLKN_3	1.37933	4.108	3.79			-7.74%
	16 CLKN_4	2.70803	3.676	3.69			0.38%
	17 CLKN_5	1.46751	3.244	3.26			0.49%
	18 CLKN_6	2.68933	2.607	2.68			2.80%
	19 CLKN_7	1.46751	2.175	2.19			0.69%
	20 CLKN_8	2.62293	1.749	2.63			50.37%



Clearance	Wiring	Timing	Costing
Clearance			
▶ Track Clearance			
▶ Via Clearance			
▶ SMD Clearance			
Same Net Gap			
SMD-Via			
Via-Via			
Pad-to-Turn Gap			
SMD-to-Turn Gap			
Buried-Via Gap			
Power Ground Plane			
Antipad Gap			



Preview DO file

OK